三路差分接收器/均衡器

概述

EL9111 和 EL9112 是三路通道差分接收器和均衡器。它们包含三个高速差分接收器，具有 5 个可编程的电极。这些电极块的输出在输出缓冲器中叠加。均衡长度由一个单独引脚上的电压设定。EL9111 和 EL9112 还包含一个三态输出，可以使多个器件并行连接，可用在多路传输的应用中。

V_{GAIN}控制信号可放大或减小增益 6dB。此外，通过给电缆提供合适的驱动，能够进一步转换 6dB的增益。

EL9111 和 EL9112 带宽 150MHz，±5V 的电源下，电流仅为 108mA。根据所需的电缆长度，一个单输入电压可用来设置合适的补偿水平。

EL9111 是 EL9112 的特殊类型，EL9112 对 EL4543 编码的三对 CAT-5 电缆上的同步信号进行译码。（详见 EL4543 的数据手册）。

EL9111 和 EL9112 采用 28 引脚 QFN 封装，规定的工作温度范围为-40°C到+85°C。

特点

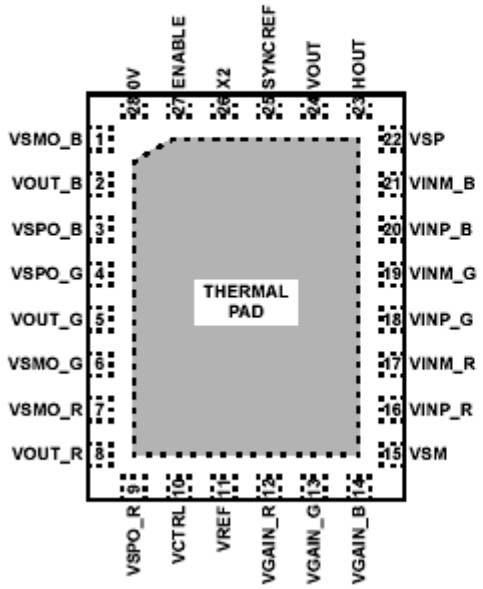
- 150MHz –3dB 带宽
- CAT-5 补偿
  - — 50MHz @ 1000 英尺
  - — 125MHz @ 500 英尺
- 108mA 电源电流
- 差分输入范围 3.2V
- 共模输入范围 -4V 到+3.5V
- ±5V 电源
- 电源低至 1.5V 有输出
- 28 引脚 QFN 封装
- 无铅封装（符合 RoHS 标准）

应用

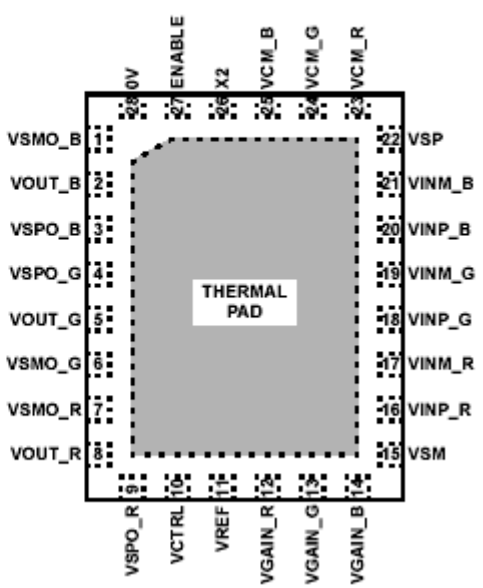
- 双绞线接收/均衡器
- KVM（键盘/视频/鼠标）
- 双绞线上传送的 VGA
- 闭路电视

引脚图

EL9111
(28-PIN QFN)
TOP VIEW



EL9112
(28-PIN QFN)
TOP VIEW



订购信息

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL9111IL	28-Pin QFN	-	MDP0046
EL9111IL-T7	28-Pin QFN	7"	MDP0046
EL9111IL-T13	28-Pin QFN	13"	MDP0046
EL9111ILZ (Note)	28-Pin QFN (Pb-Free)	-	MDP0046
EL9111ILZ-T7 (Note)	28-Pin QFN (Pb-Free)	7"	MDP0046
EL9111ILZ-T13 (Note)	28-Pin QFN (Pb-Free)	13"	MDP0046

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL9112IL	28-Pin QFN	-	MDP0046
EL9112IL-T7	28-Pin QFN	7"	MDP0046
EL9112IL-T13	28-Pin QFN	13"	MDP0046
EL9112ILZ (Note)	28-Pin QFN (Pb-Free)	-	MDP0046
EL9112ILZ-T7 (Note)	28-Pin QFN (Pb-Free)	7"	MDP0046
EL9112ILZ-T13 (Note)	28-Pin QFN (Pb-Free)	13"	MDP0046

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

极限参数（T_A=25℃）

电源电压V_S^+到V_S^- …… 12V
每通道上最大连续输出电流 …… 30mA
功耗 …… 见曲线图
引脚电压……V_S- -0.5V 到V_S+ +0.5V
储存温度…… -65℃到+150℃
工作环境温度……-40℃到+85℃
晶片节点温度…… 150℃

注意：强度超出所列的极限参数可能导致器件的永久性损坏。这些仅仅是极限参数，并不意味着在极限条件下或在任何其它超出推荐工作条件所示参数的情况下器件能有效工作。

重要提示：所有具有最小/最大值的参数都是有保证的。典型值仅作为信息提供。除非另有说明，所有的测试都在规定的温度下进行，且为脉冲测试，因此：$T_J=T_C=T_A$。

电气指标

$V_{SA}+=V_A+=+5V$，$V_{SA}-=V_A-=-5V$，$T_A= 25℃$，除非另有说明。

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	Bandwidth	(See Figure 1)		150		MHz
SR	Slew Rate	V_{IN} = -1V to +1V, V_G = 0.39, V_C = 0, R_L = 75 + 75Ω		1.5		kV/µs
THD	Total Harmonic Distortion	10MHz $2V_{P-P}$ out, V_G = 1V, X2 gain, V_C = 0		-50		dBc
DC PERFORMANCE						
$V(V_{OUT})_{OS}$	Offset Voltage	X2 = high, no equalization	-110	-10	+78	mV
ΔV_{OS}	Channel-to-Channel Offset Matching	X2 = high, no equalization	-100	0	+100	mV
INPUT CHARACTERISTICS						
CMIR	Common-mode Input Range			-4/+3.5		V
O_{NOISE}	Output Noise	V_G = 0V, V_C = 0V, X2 = HIGH, R_{LOAD} = 150Ω, Input 50Ω to GND, 10MHz		-110		dBm
CMRR	Common-mode Rejection Ratio	Measured at 10kHz		-80		dB
CMRR	Common-mode Rejection Ratio	Measured at 10MHz		-55		dB
CMBW	CM Amplifier Bandwidth	10K || 10pF load		50		MHz
CM_{SLEW}	CM Slew Rate	Measured @ +1V to -1V		100		V/µs
C_{INDIFF}	Differential Input Capacitance	Capacitance V_{INP} to V_{INM}		600		fF
R_{INDIFF}	Differential Input Resistance	Resistance V_{INP} to V_{INM}	1	2.4		MΩ
C_{INCM}	CM Input Capacitance	Capacitance V_{INP} = V_{INM} to GND		1.2		pF
R_{INCM}	CM Input Resistance	Resistance V_{INP} = V_{INM} to GND	1	2.8		MΩ
$+I_{IN}$	Positive Input Current	DC bias @ V_{INP} = V_{INM} = 0V		1		µA
$-I_{IN}$	Negative Input Current	DC bias @ V_{INP} = V_{INM} = 0V		1		µA
V_{INDIFF}	Differential Input Range	V_{INP} - V_{INM} when slope gain falls to 0.9	2.5	3.2		V
OUTPUT CHARACTERISTICS						
$V(V_{OUT})$	Output Voltage Swing	R_L = 150Ω		±3.5		V
$I(V_{OUT})$	Output Drive Current	R_L = 10Ω, V_{INP} = 1V, V_{INM} = 0V, X2 = high, V_G = 0.39	50	60		mA
$R(V_{CM})$	CM Output Resistance of VCM_R/G/B (EL9112 only)	at 100kHz		30		Ω
Gain	Gain	V_C = 0, V_G = 0.39, X2 = 5, R_L = 150Ω	0.85	1.0	1.1	
ΔGain	Channel-to-Channel Gain Matching	V_C = 0, V_G = 0.39, X2 = 5, R_L = 150Ω		3	6	%
$V(SYNC)_{HI}$	High Level output on V/H_{OUT} (EL9111 only)		$V(V_{SP})$ - 0.1V		$V(V_{SP})$	

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$V(SYNC)_{LO}$	Low Level output on V/H_{OUT} (EL9111 only)		0		V(SYNC REF) + 0.1V	
SUPPLY						
I_{SON}	Supply Current per Channel	V_{ENBL} = 5, V_{INM} = 0	32	36	39	mA
I_{SOFF}	Supply Current per Channel	V_{ENBL} = 0, V_{INM} = 0	0.2		0.4	mA
PSRR	Power Supply Rejection Ratio	DC to 100kHz, ±5V supply		65		dB
LOGIC CONTROL PINS (ENABLE, X2)						
V_{HI}	Logic High Level	V_{IN} - V_{LOGIC} ref for guaranteed high level	1.35			V
V_{LOW}	Logic Low Level	V_{IN} - V_{LOGIC} ref for guaranteed low level			0.8	V
I_{LOGICH}	Logic High Input Current	V_{IN} = 5V, V_{LOGIC} = 0V			50	µA
I_{LOGICL}	Logic Low Input Current	V_{IN} = 0V, V_{LOGIC} = 0V			15	µA

引脚描述

PIN NUMBER	EL9111IL PIN NAME	EL9111IL PIN FUNCTION	EL9112IL PIN NAME	EL9112IL PIN FUNCTION
1	VSMO_B	-5V to blue output buffer	VSMO_B	-5V to blue output buffer
2	VOUT_B	Blue output voltage referenced to 0V pin	VOUT_B	Blue output voltage referenced to 0V pin
3	VSPO_B	+5V to blue output buffer	VSPO_B	+5V to blue output buffer
4	VSPO_G	+5V to green output buffer	VSPO_G	+5V to green output buffer
5	VOUT_G	Green output voltage referenced to 0V pin	VOUT_G	Green output voltage referenced to 0V pin
6	VSMO_G	-5V to green output buffer	VSMO_G	-5V to green output buffer
7	VSMO_R	-5V to red output buffer	VSMO_R	-5V to red output buffer
8	VOUT_R	Red output voltage referenced to 0V pin	VOUT_R	Red output voltage referenced to 0V pin
9	VSPO_R	+5V to red output buffer	VSPO_R	+5V to red output buffer
10	VCTRL	Equalization control voltage (0V to 1V)	VCTRL	Equalization control voltage (0V to 1V)
11	VREF	Reference voltage for logic signals, V_{CTRL} and V_{GAIN} pins	VREF	Reference voltage for logic signals, V_{CTRL} and V_{GAIN} pins
12	VGAIN_R	Red channel gain voltage (0V to 1V)	VGAIN_R	Red channel gain voltage (0V to 1V)
13	VGAIN_G	Green channel gain voltage (0V to 1V)	VGAIN_G	Green channel gain voltage (0V to 1V)
14	VGAIN_B	Blue channel gain voltage (0V to 1V)	VGAIN_B	Blue channel gain voltage (0V to 1V)
15	VSM	-5V to core of chip	VSM	-5V to core of chip
16	VINP_R	Red positive differential input	VINP_R	Red positive differential input
17	VINM_R	Red negative differential input	VINM_R	Red negative differential input
18	VINP_G	Green positive differential input	VINP_G	Green positive differential input
19	VINM_G	Green negative differential input	VINM_G	Green negative differential input
20	VINP_B	Blue positive differential input	VINP_B	Blue positive differential input
21	VINM_B	Blue negative differential input	VINM_B	Blue negative differential input
22	VSP	+5V to core of chip	VSP	+5V to core of chip
23	HOUT	Decoded Horizontal sync referenced to SYNCREF	VCM_R	Red common-mode voltage at inputs
24	VOUT	Decoded Vertical sync referenced to SYNCREF	VCM_G	Green common-mode voltage at inputs
25	SYNCREF	Reference level for H_{OUT} and V_{OUT} logic outputs	VCM_B	Blue common-mode voltage at inputs

26	X2	Logic signal for x1/x2 output gain setting	X2	Logic signal for x1/x2 output gain setting
27	ENABLE	Chip enable logic signal	ENABLE	Chip enable logic signal
28	0V	0V reference for output voltage	0V	0V reference for output voltage

典型性能特征曲线图

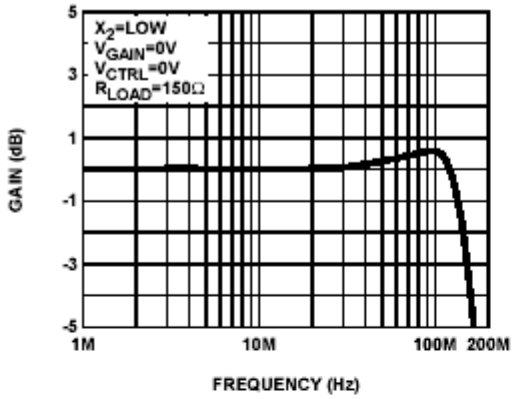


FIGURE 1. FREQUENCY RESPONSE OF ALL CHANNELS

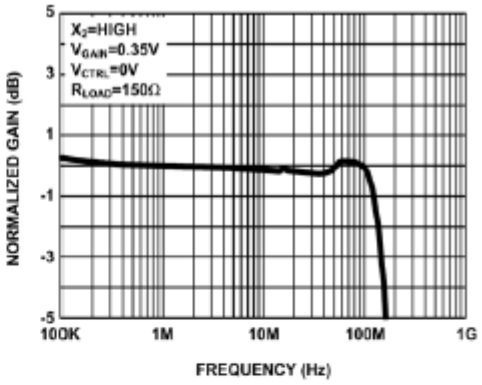


FIGURE 2. GAIN vs FREQUENCY ALL CHANNELS

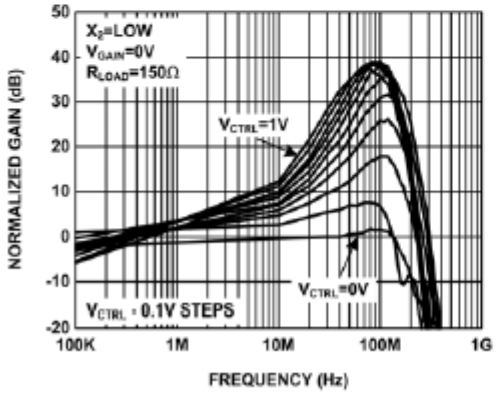


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS V_{CTRL}

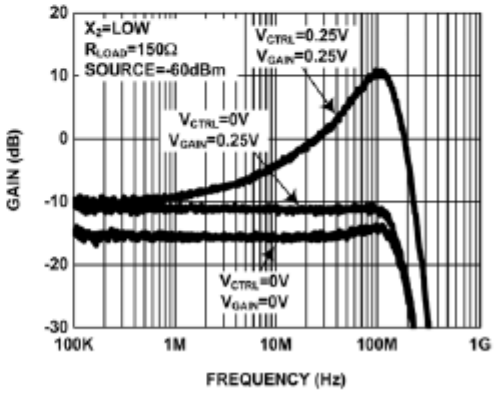


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS V_{CTRL} & V_{GAIN}

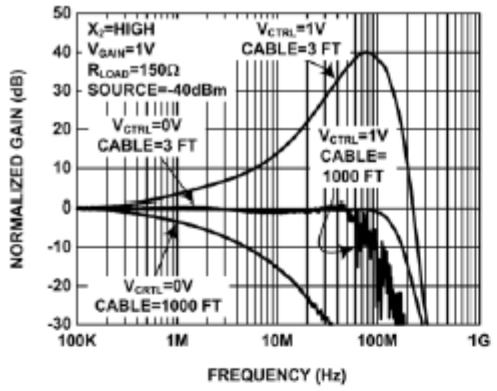


FIGURE 5. GAIN vs FREQUENCY FOR VARIOUS V_{CTRL} & CABLE LENGTHS

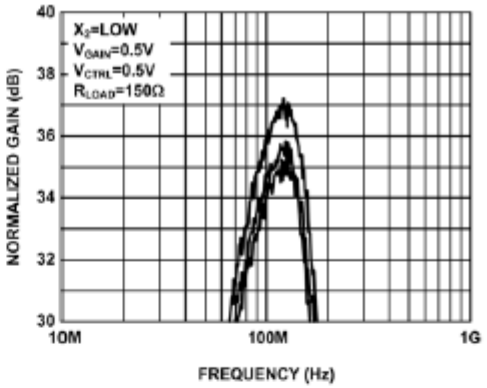


FIGURE 6. CHANNEL MISMATCH

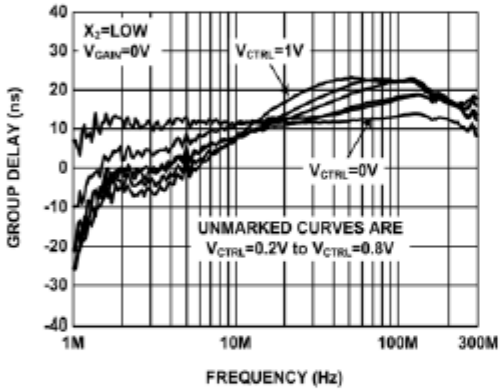


FIGURE 7. GROUP DELAY vs FREQUENCY FOR VARIOUS V_{CTRL}

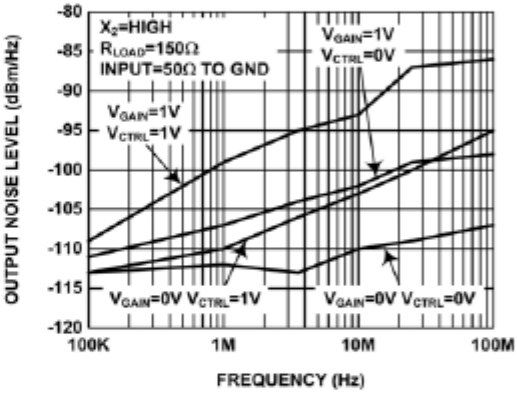


FIGURE 8. OUTPUT NOISE

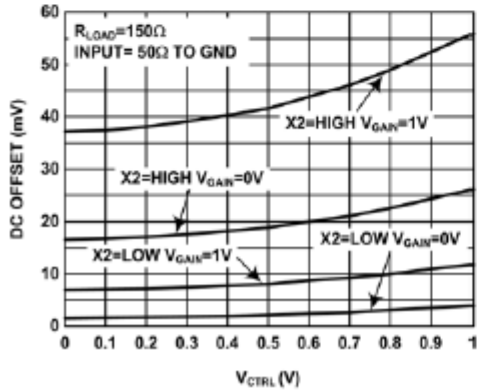


FIGURE 9. OFFSET vs V_{CTRL}

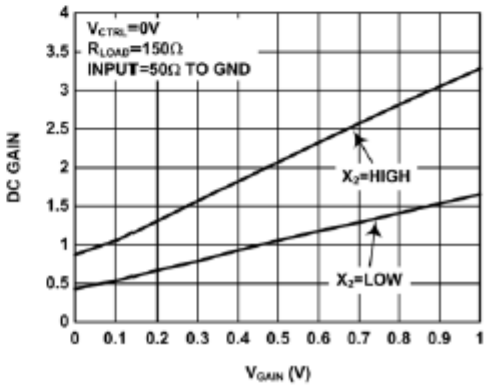


FIGURE 10. DC GAIN vs V_{GAIN}

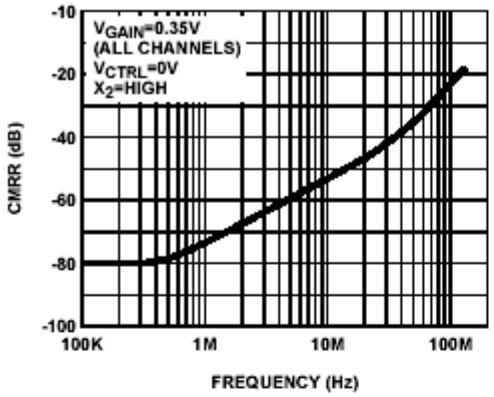


FIGURE 11. COMMON-MODE REJECTION

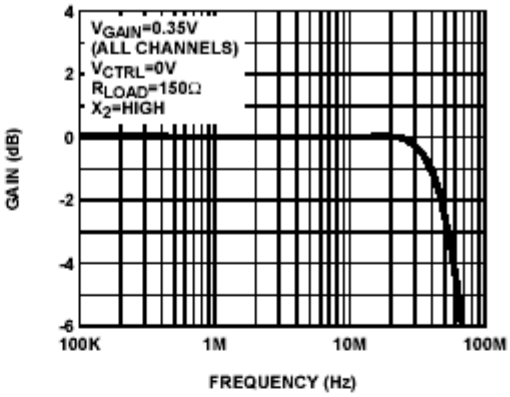


FIGURE 12. CM AMPLIFIER BANDWIDTH

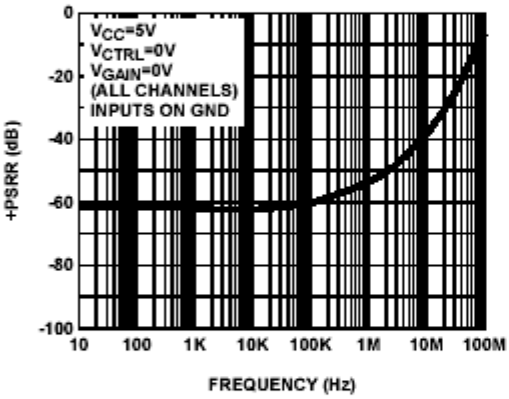


FIGURE 13. (+)PSRR vs FREQUENCY

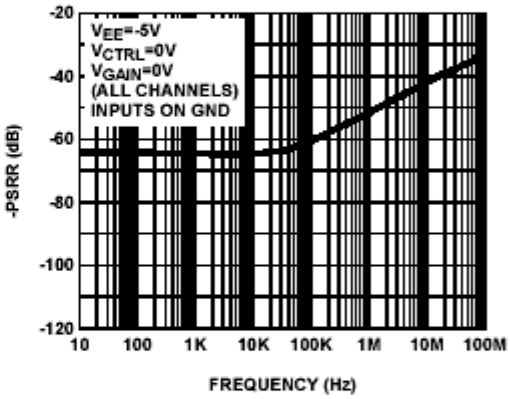


FIGURE 14. (-)PSRR vs FREQUENCY

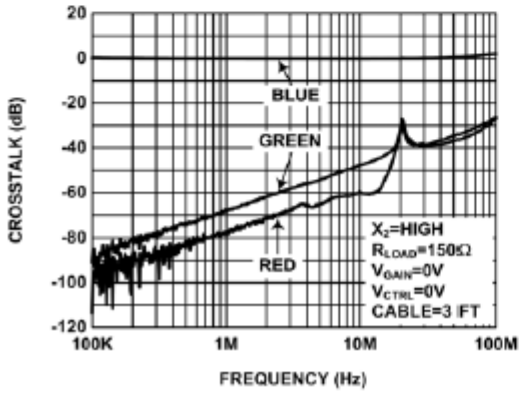


FIGURE 15. BLUE CROSSTALK

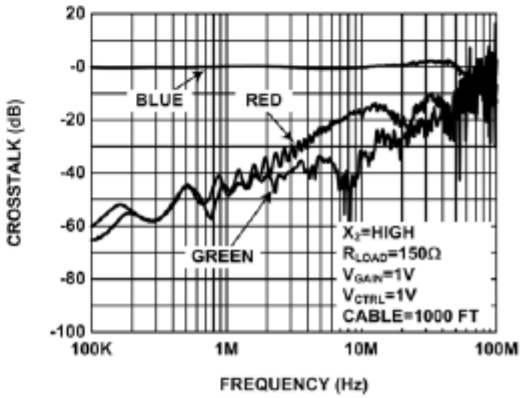


FIGURE 16. BLUE CROSSTALK

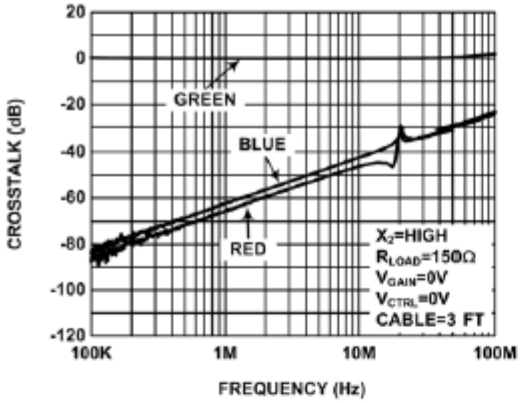


FIGURE 17. GREEN CROSSTALK

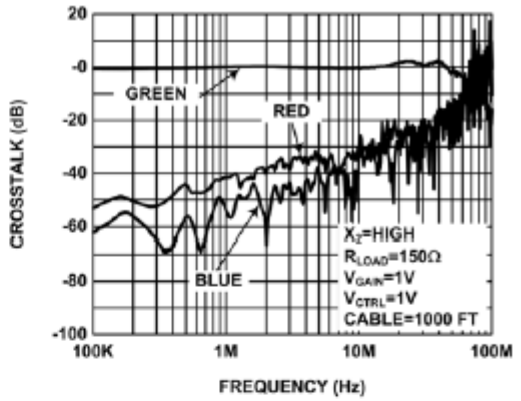


FIGURE 18. GREEN CROSSTALK

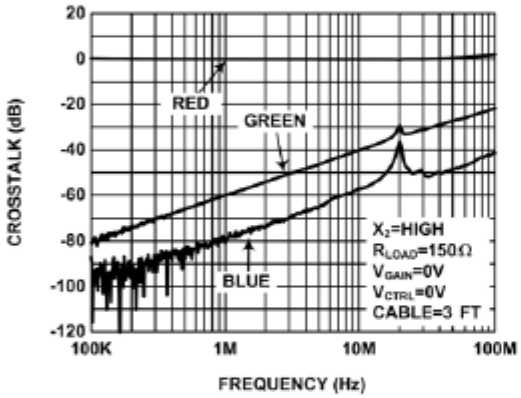


FIGURE 19. RED CROSSTALK

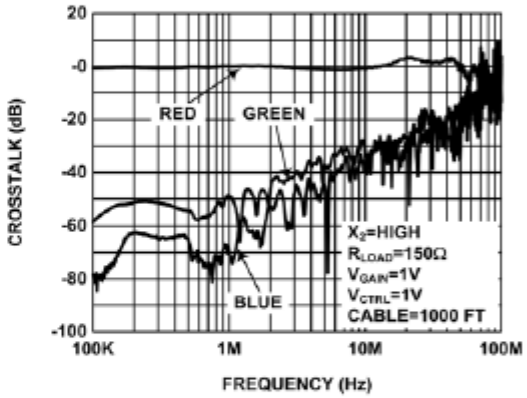


FIGURE 20. RED CROSSTALK

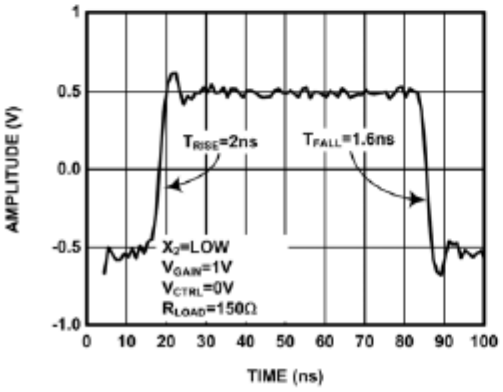


FIGURE 21. RISE TIME AND FALL TIME

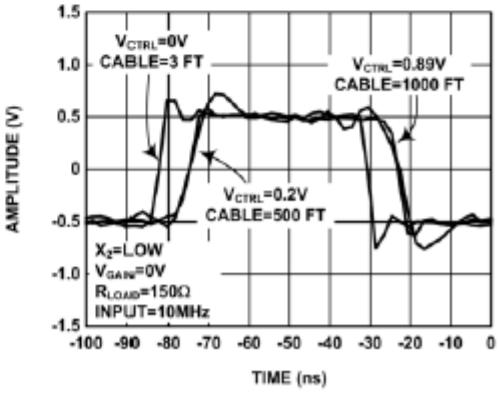


FIGURE 22. PULSE RESPONSE FOR VARIOUS CABLE LENGTHS

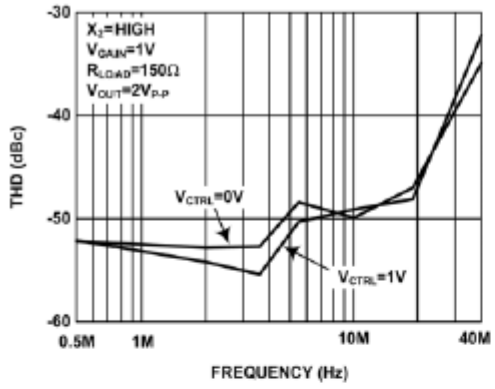


FIGURE 23. TOTAL HARMONIC DISTORTION

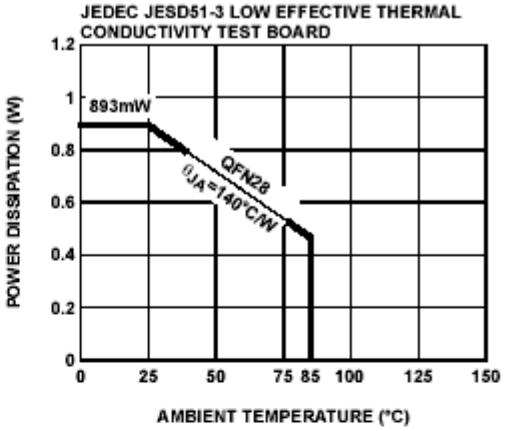


FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

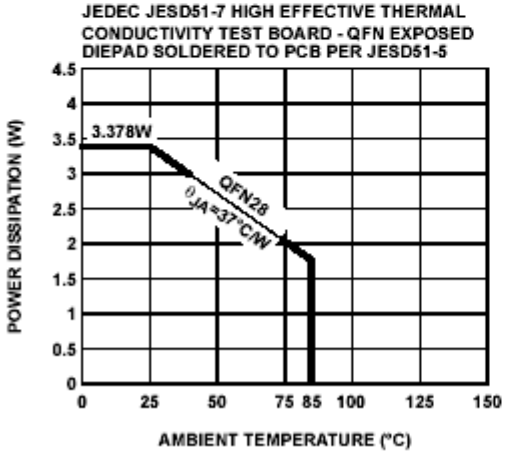


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

应用信息

逻辑控制

EL9112 有两个逻辑输入引脚：芯片使能（ENBL）和开关增益（X2）。逻辑电路在逻辑基准管脚（VREF）的电势之上都有 1.1V 的额定门限。在大多数应用中，芯片都工作在+5V，0V，-5V 的供电系统下，逻辑值在 0V 和+5V 之间。在这种情况下，逻辑基准电压应工作在 0V 电源下。如果逻辑以-5V 电源为参考，则逻辑基准应接-5V。逻辑基准管脚的电流约为 60μA，如果输入为真（正的），电流还会升至大约 200μA 。

当保持在逻辑基准电平时，逻辑输入都达到 10μA。当为正时，输入吸收了随高电平而定的电流，该电流在高于基准电平 5V 的高电平下，可达 50μA。

不使用时，逻辑输入应接合适的电压，以确定它们的状态。

控制基准和信号基准

我们需要模拟控制电压来设置均衡器和对比度。这些信号是以控制基准引脚为参考，范围在 0V-1V 的电压。一般控制基准脚接 0V，控制电压从 0V 到 1V 变化。但是，也允许将控制基准接-5V 和 0V 间的任意电势，控制电压以该电势为参考。

控制电压脚本身有高阻抗。控制基准脚的电流在 0μA 到 200μA 之间，由应用的控制电压决定。

控制基准和逻辑基准有效地避免了必须选择 0V，和仅仅只能工作在±5V（或 0V 到 10V）的情况。然而，我们还需要一个基准来定义单终端输出信号的 0V 电平。输出信号的基准由 0V 管脚提供。输出级不能完全上拉或下拉任一电源，因此，基准必须被定位在允许输出的整个范围内。当该脚上的任何噪声直接转移到输出时，0V 基准应该连接到“安静的地面”。0V 管脚具有高阻抗，可吸收几μA 的直流偏置电流，也可吸收相似水平的交流电流。

均衡

当通过双绞线传送一个信号时，高频信息（约 1MHz）比低频信息衰减得更厉害。衰减主要是由电阻的表面效应损失，和随导线的电阻率，金属丝的表面条件和直径变化的损失曲线决定的。对以 24awg 铜线（Cat 5 etc.）为芯的高性能双绞线，不同电缆类型的这些参数变化非常小，一般的电缆会表现出同样的频率损失。（较低损失的电缆可以和较长的有较高损失的电缆相比较）。这使得 EL9112 具有唯一的均衡公式。

加在管脚V_{CTRL}和V_{REF}之间一个控制电压，公式决定的频率如图 8 所示。电缆损失达到约 100MHz。在此之上，系统增益迅速增加以降低噪声带宽。对更高的控制电压，增加更快，因此，系统（电缆+均衡器）带宽随电缆长度的增加而减少。这是理想的，因为随均衡的增加，噪声成为一个递增的量。

对比度

通过改变管脚V_{GAIN}和V_{REF}之间的电压，信号通路的增益可按 4：1 的比例变化。增益的改变与控制电压几乎呈线性变化。正常工作下，一般选择X2 模式，输出负载与其相配。在大约 0.35V的增益控制电压下将达到输出负载的单元增益。这使得增益可以升高或降低 6dB来补偿影响视频信号对比度的增益/损失的误差。图 26 展示了增益控制电压下负载增益曲线的例子。

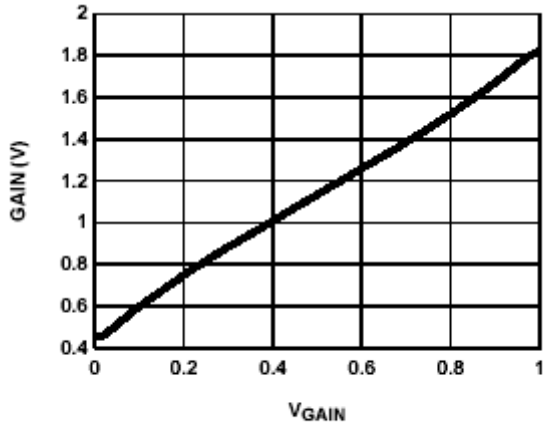


FIGURE 26. VARIATION OF GAIN WITH GAIN CONTROL VOLTAGE

共模同步译码

EL9111 的特点是共模译码，可对水平的和垂直方向上的信息进行译码，该信息由 EL4543 的三个差分输入端编码。因此，仅使用三对电缆，完整的 RGB 视频信号和相关的同步信息即可被传送。

编码是基于 EL4543 的编码图，如图 27 和表 1 所示。该图是一个三级体系，共模电压的总和产生固定的直流电均值，没有交流电的成分。这样就消除了电磁辐射干扰对双绞线上共模信号的影响。

共模电压最初由EL9111 的三个输入产生，然后被传递到内部逻辑译码电路，提供水平和垂直方向上的同步输出信号（H_{OUT}和V_{OUT}）。

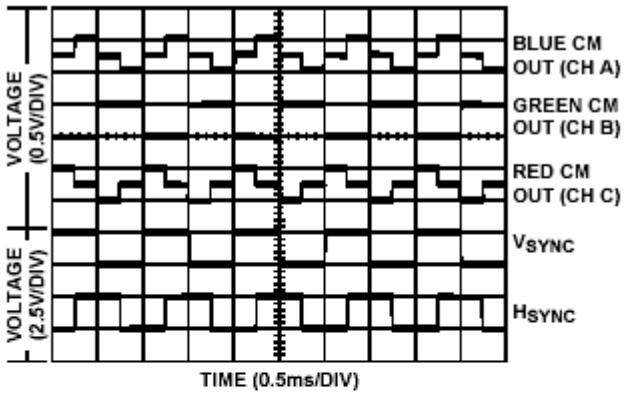


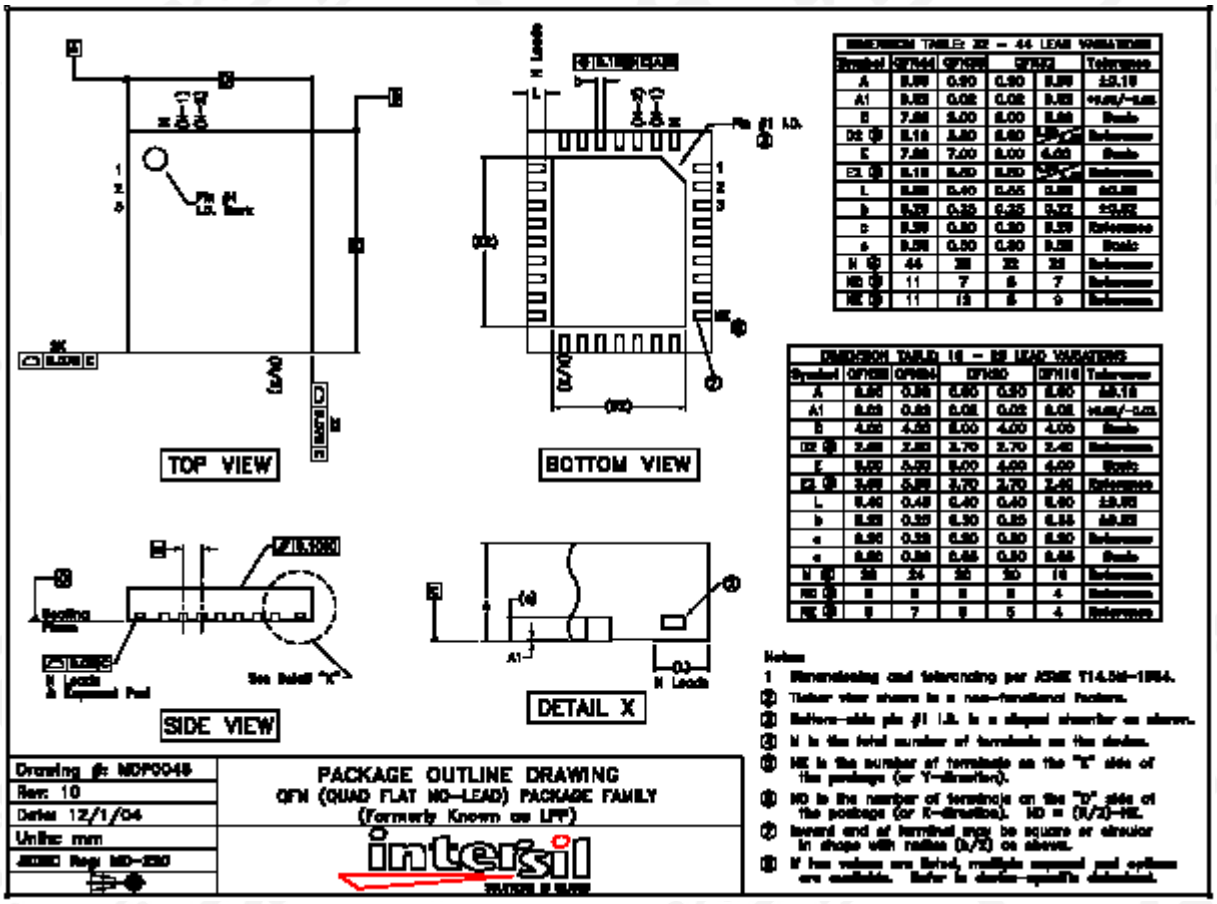
FIGURE 27. H & V SYNCS ENCODED

TABLE 1. H AND V SYNC DECODING

RED CM	GREEN CM	BLUE CM	H_{SYNC}	V_{SYNC}
Mid	High	Low	Low	Low
High	Low	Mid	Low	High
Low	High	Mid	High	Low
Mid	Low	High	High	High

NOTE: Level 'Mid' is halfway between 'High' and 'Low'

封装轮廓图



注：此图可能不是最新的版本。要查找最新的版本，请登陆 Intersil 的网站：
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